From performance validation to volume introduction of ASML's NXE platform

SEMICON West, July 2012

Hans Meiling

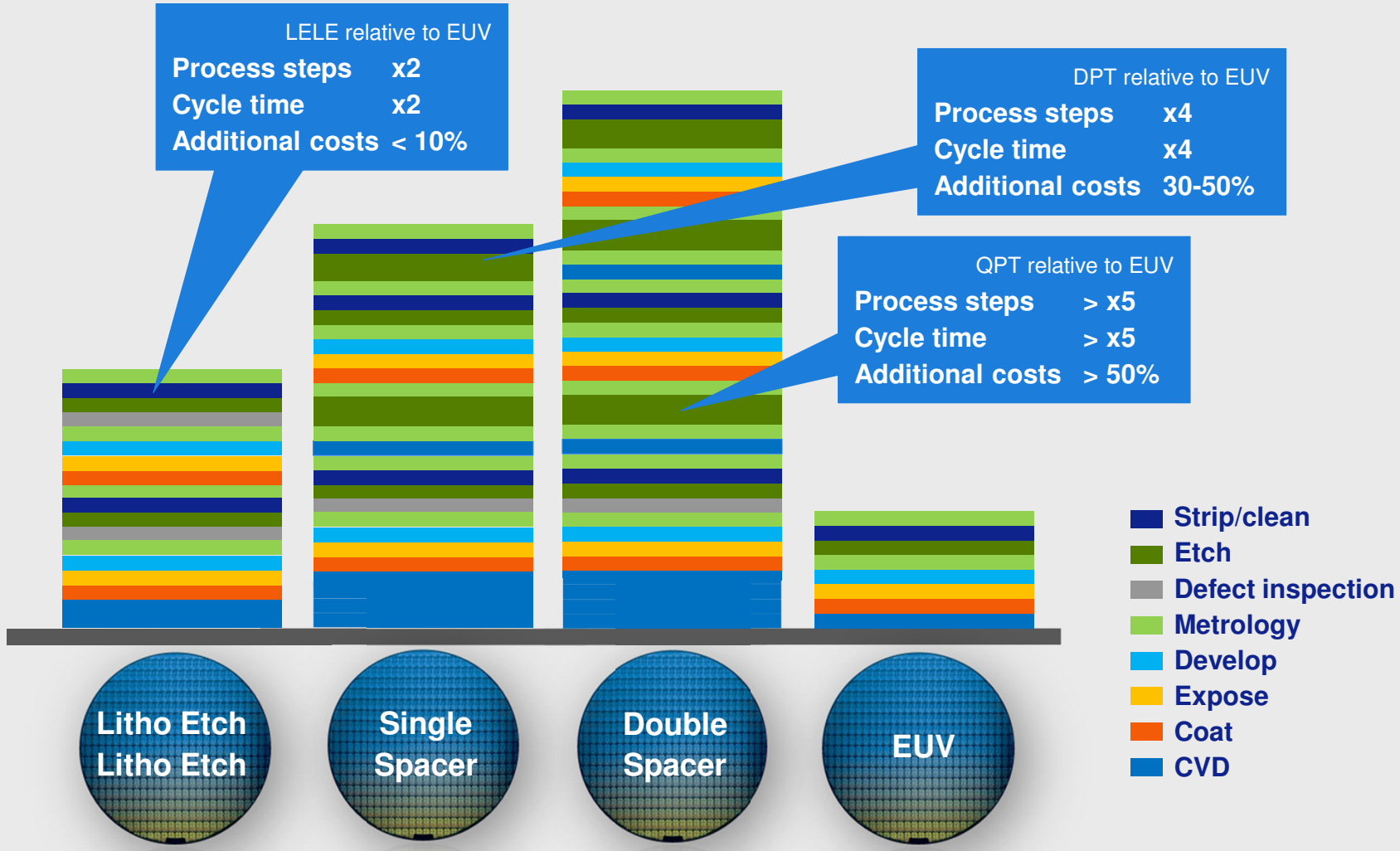
Acknowledgements

The work presented is result of a large team at ASML and our technology partners.

Content

- Why EUVL
- ASML EUV product roadmap
  - NXE:3100
  - NXE:3300
- Roadmap Extendibility

EUVL simplifies process and reduces cost



Data is based on Customer interaction

ASML

EUV lithography product development extends >25 years

1st publications EUV lithography (LLNL, Bell Labs, Japan)

ASML starts EUVL research program

ASML ships 2 alpha demo tools: IMEC (Belgium) and CNSE (USA)

ASML ships 1st pre-production tool

'84 '85 '86 '87 '88 '89 '90 '91 '92 '93 '94 '95 '96 '97 '98 '99 '00 '01 '02 '03 '04 '05 '06 '07 '08 '09 '10 '11 '12

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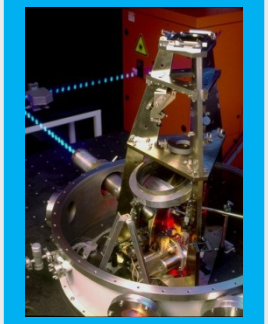

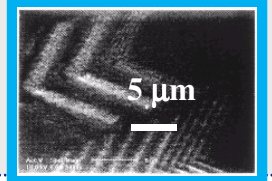

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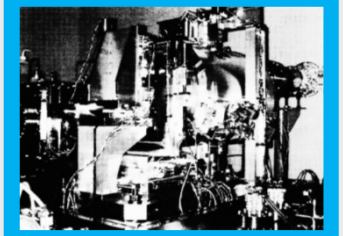

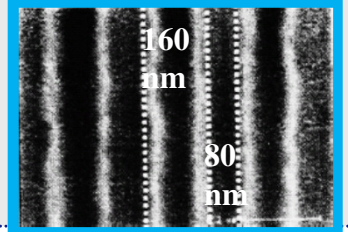

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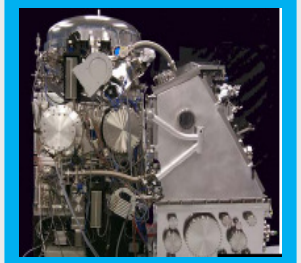

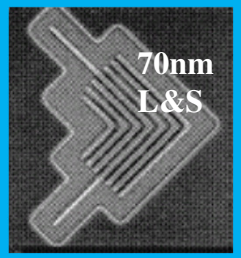

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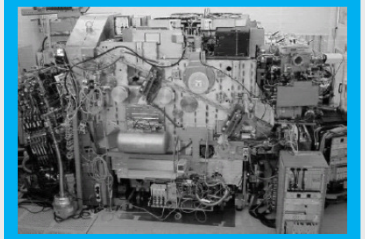

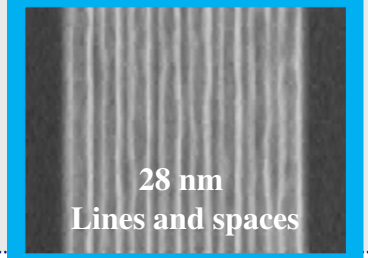

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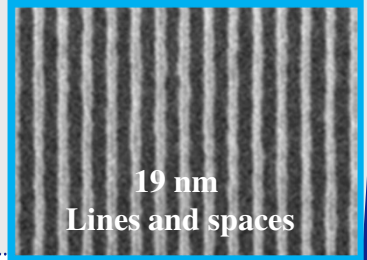

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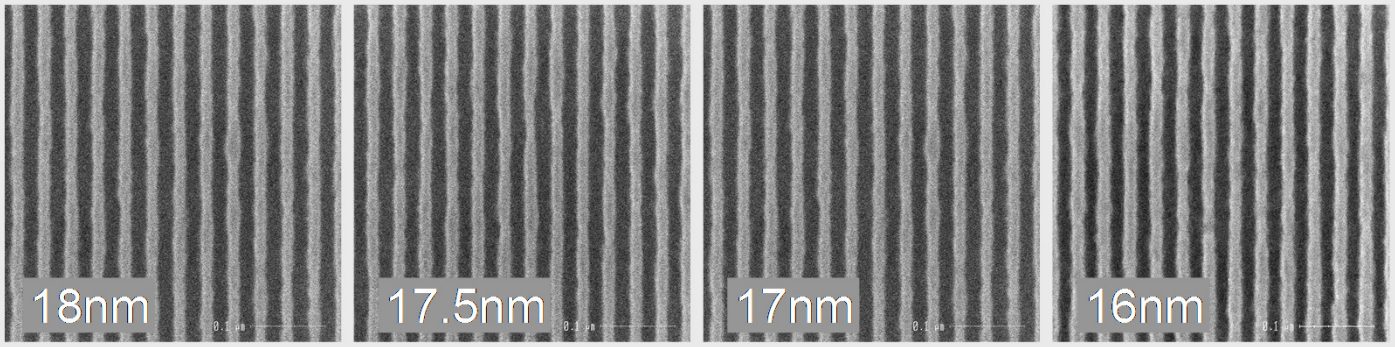
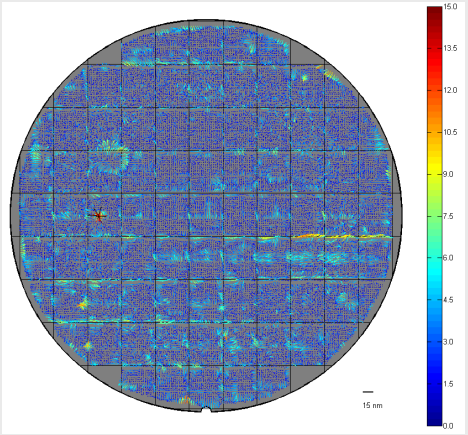
>10 years Imaging and Overlay progress summarized

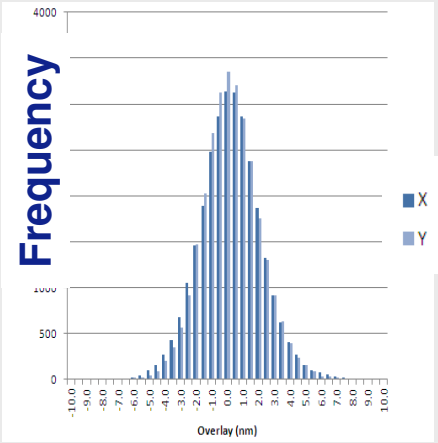
Source: IMEC



Exposed on an NXE:3100 with dipole-30x, exposure dose 33mJ/cm^2

Source: IMEC





XT:1900Gi to NXE:3100 matched overlay. 3σ:X = 6.0nm, Y = 5.6nm

ASML

NXE:3100's are exposing wafers in fabs worldwide

System 1
Exposing wafers for device development

System 2
Exposing wafers for device development

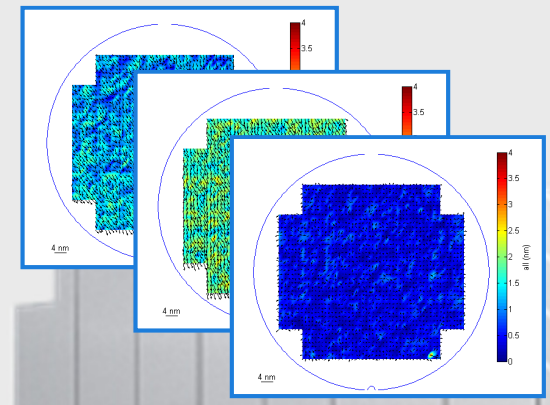
System 3:
Exposing wafers for device development

System 4:
Exposing wafers for device development

System 5:
Exposing wafers for device development

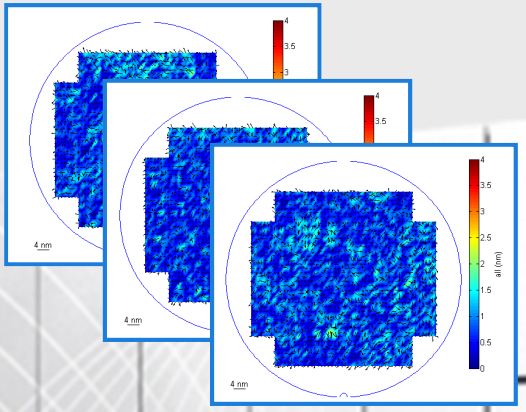
System 6:
Exposing wafers for device development

Overlay – consistent SCO <~2nm on all six NXE:3100's has been achieved



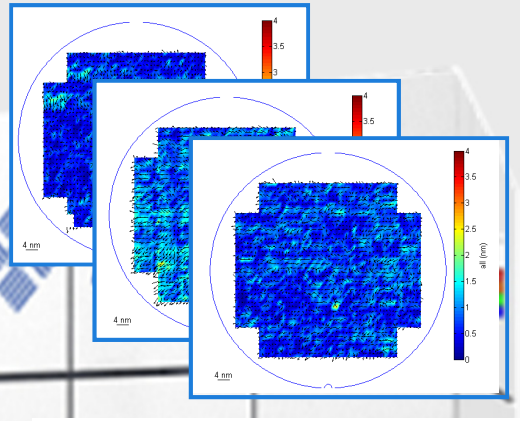
System A

(1.0,1.4) (1.0,2.1) (0.7,0.4)



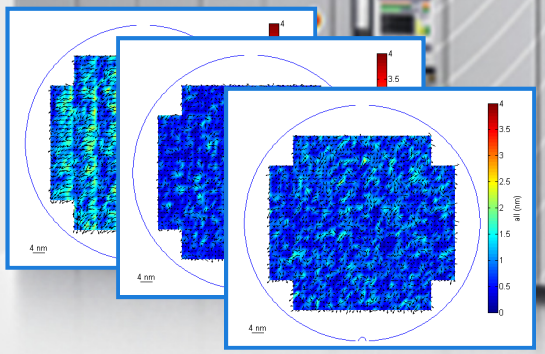
System B

(1.1,0.7) (1.0,0.9) (0.9, 1.0)



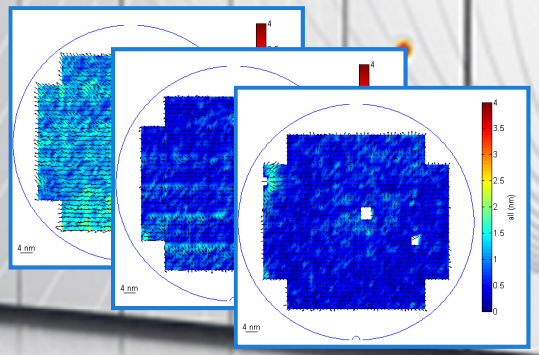
System C

(0.7,1.2) (1.5,1.2) (1.1,0.8)



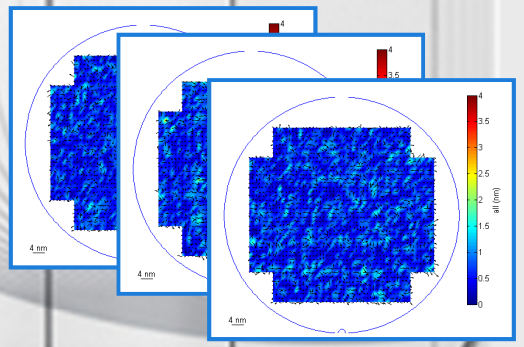
System D

(1.8,1.0) (0.7,0.7) (0.5,0.9)



System E

(1.8,0.9) (1.0,1.2) (1.0,0.9)



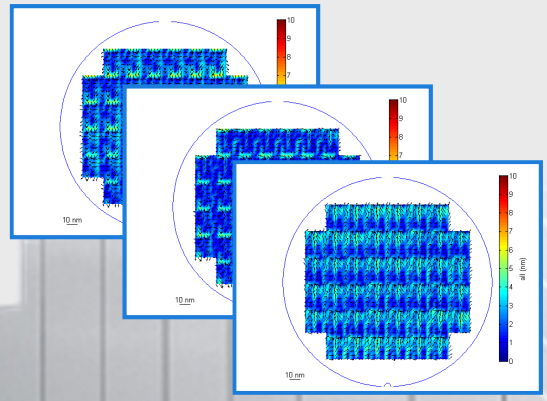
System F

(1.1,0.7) (0.9,0.6) (0.9,0.7)

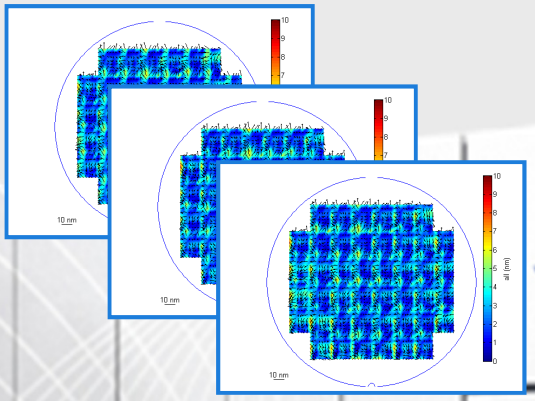
SCO = single-chuck overlay

ASML

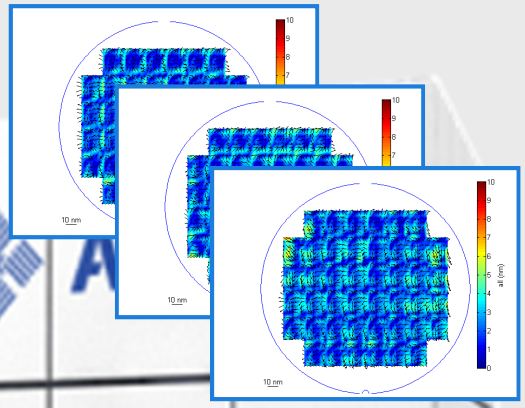
Overlay – consistent MMO <6.5nm on all six NXE:3100's has been achieved



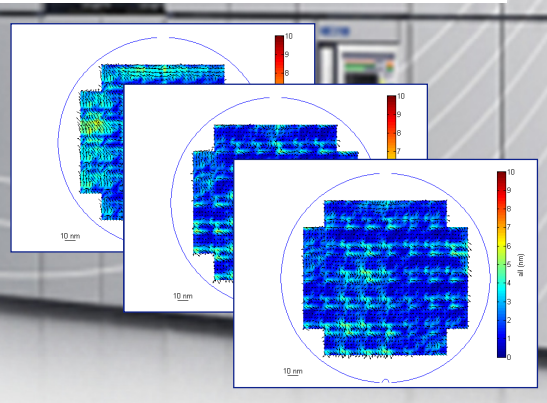
System A
(4.0,6.3) (4.3,5.0) (4.3,5.0)



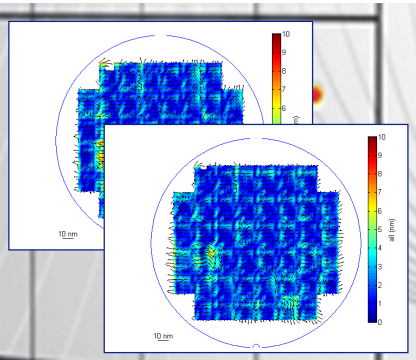
System B
(4.5,6.0) (4.3,6.1) (4.9,6.3)



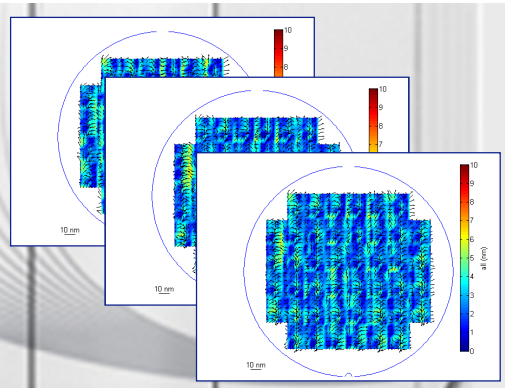
System C
(5.3,4.0) (5.5,5.0) (5.5,5.5)



System D
(4.6,5.1) (5.2,5.8) (4.7,4.5)



System E
(6.2,4.9) (6.1,4.3)



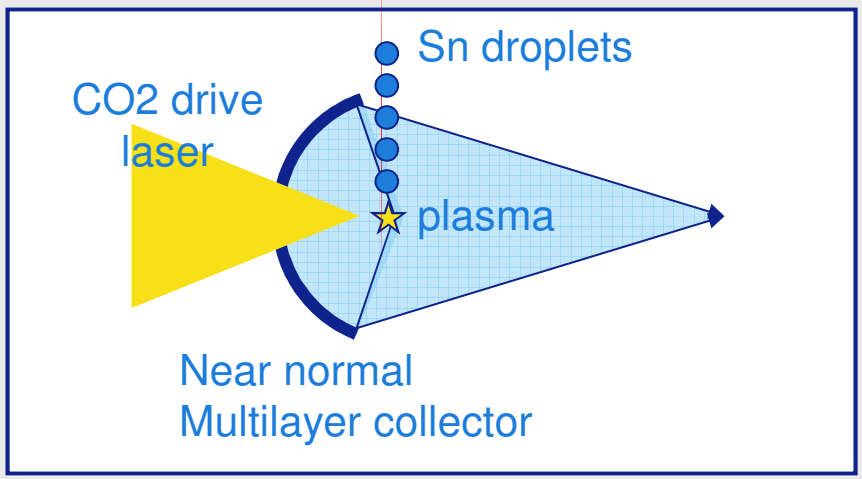
System F
(5.7,6.2) (5.7,5.5) (5.4,5.9)

MMO (matched machine overlay) to XT:1400-based reference wafer

ASML

Two EUV source concepts integrated and exposing wafers

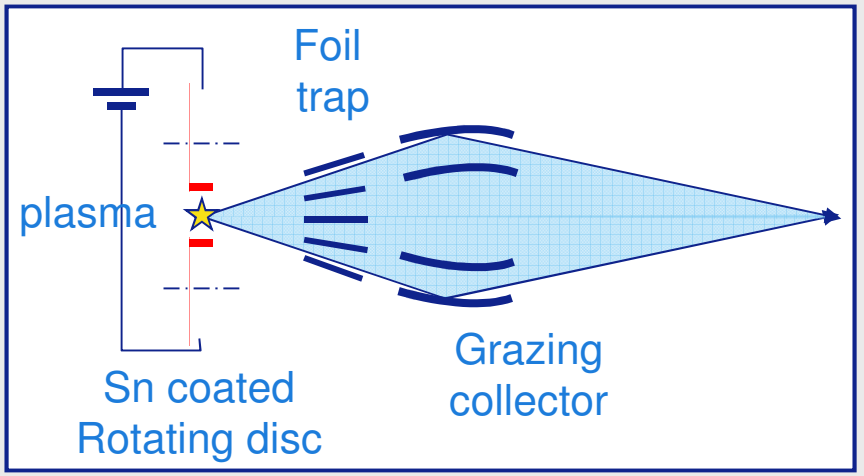
Laser-Produced Plasma (LPP)



- CO_2 laser ignites tin plasma
- Debris mitigation by background gas and possible magnetic field

Suppliers: Cymer, Gigaphoton

Laser-assisted Discharge Plasma (LDP)



- High voltage ignites tin plasma
- Debris mitigation by rotating foil trap

Supplier: Xtreme Technologies

ASML

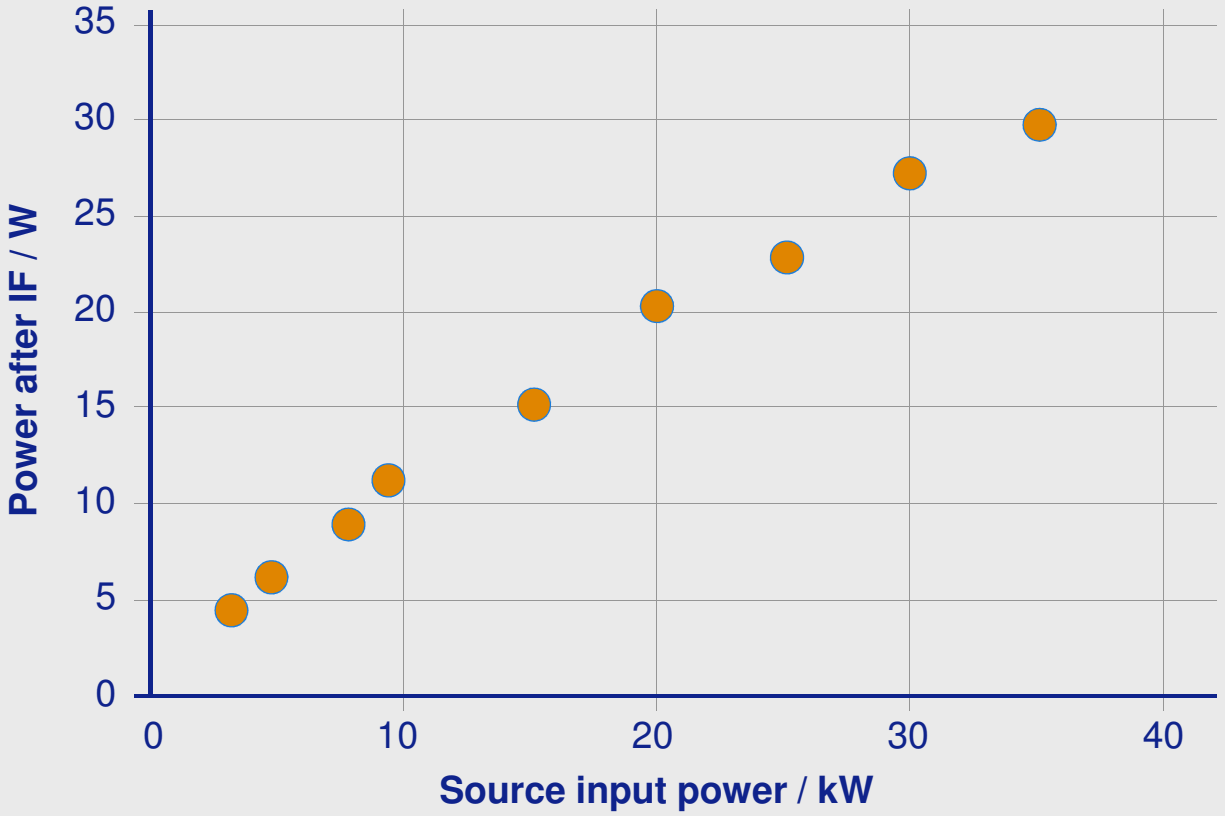
XTREME/USHIO LDP Source: 5-7W

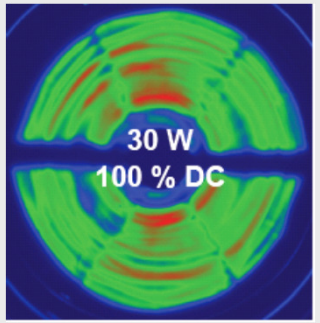
USHIO/XTREME 3100 source used for integration of 3300 at ASML

- One year ago 1 USHIO/XTREME source was integrated in 3100 scanner at customer Current power 5-7W
- Today we have 2 USHIO/XTREME sources running at IMEC and ASML at about 5-7W
- Scaling capability to >25W demonstrated

ASML

LDP source capability up to ~30 W demonstrated





Xtreme Technologies, SPIE 2012

ASML

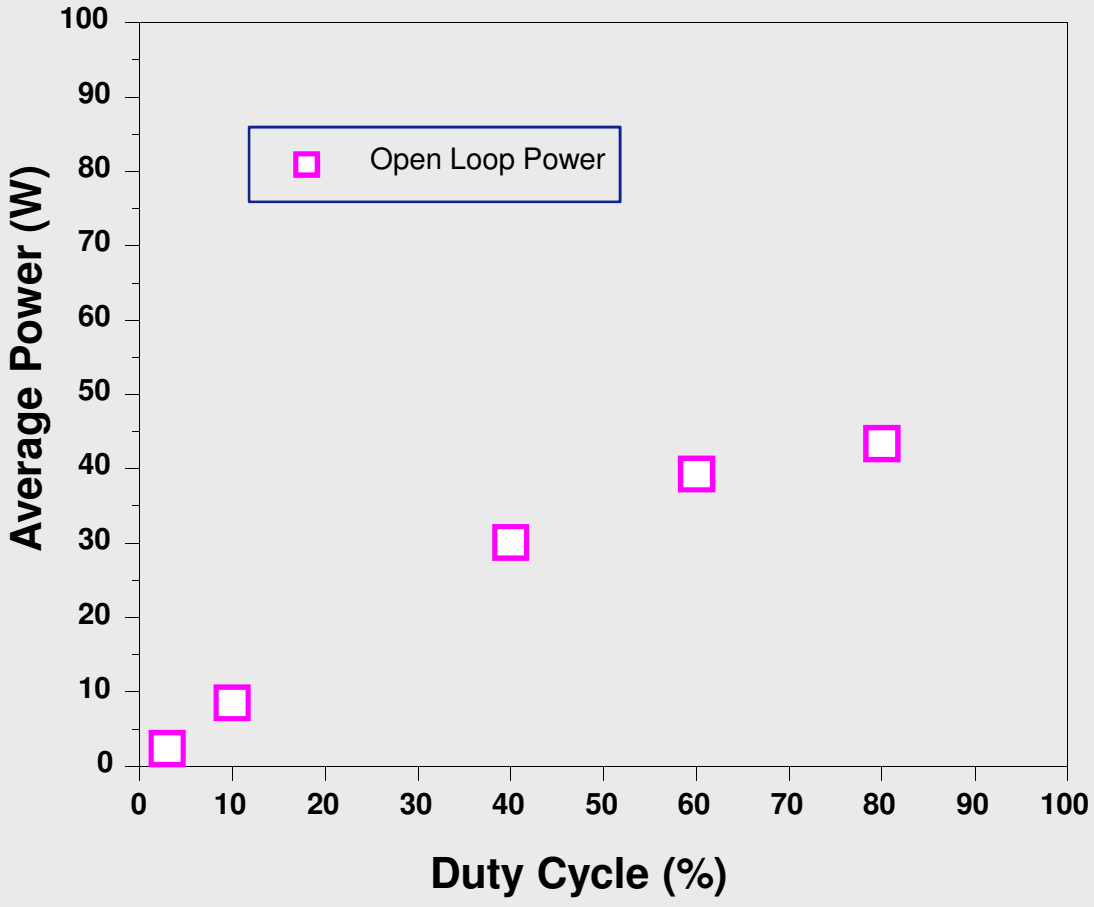
Cymer LPP sources at 5 customer sites operate at about 10 W

Cymer 3300 hybrid source installed at ASML for 3300 integration

- One year ago, 4 Cymer LPP EUV sources were integrated in 3100 scanners at customers and running at 1-2W.
- Today we have 5 Cymer 3100 LPP sources running at customers at about 10 W.
- In addition, 4 3100 sources are at Cymer and ASML for continued development and 1 Cymer 3300 LPP hybrid source is at ASML for NXE:3300B integration.

ASML

Cymer LPP: MOPA-PrePulse average EUV power up to ~50 W achieved

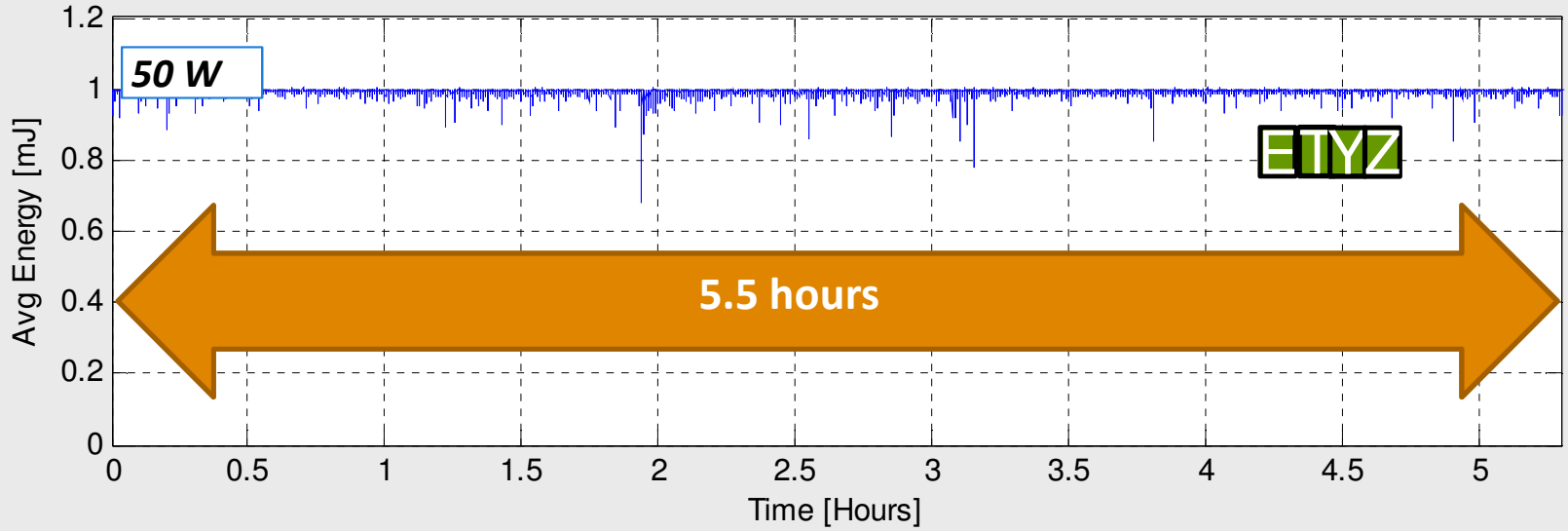


Source: Cymer

- Over 90W in-burst power achieved at low duty cycle
- Current focus is on maintaining in-burst power at high duty cycle

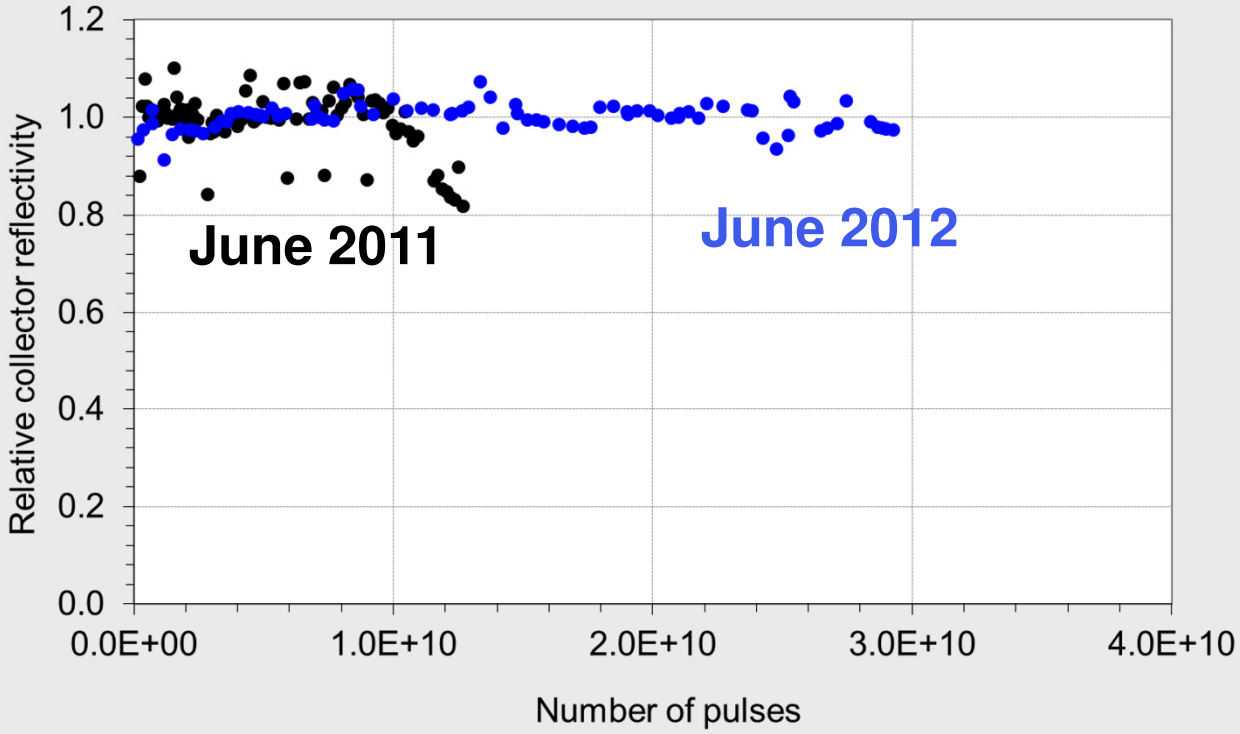
Cymer LPP: MOPA-PrePulse closed loop control over 5 hours achieved

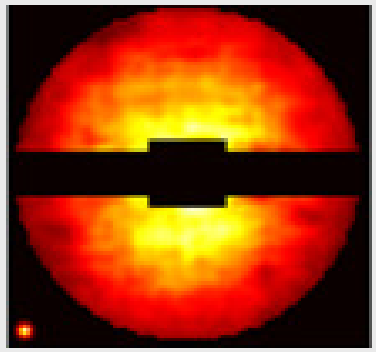
50W in-burst dose-controlled power at 40% duty cycle
Energy, timing, and position under closed loop control



Source: Cymer

Cymer collector shows stable reflectivity over more than 30 billion pulses



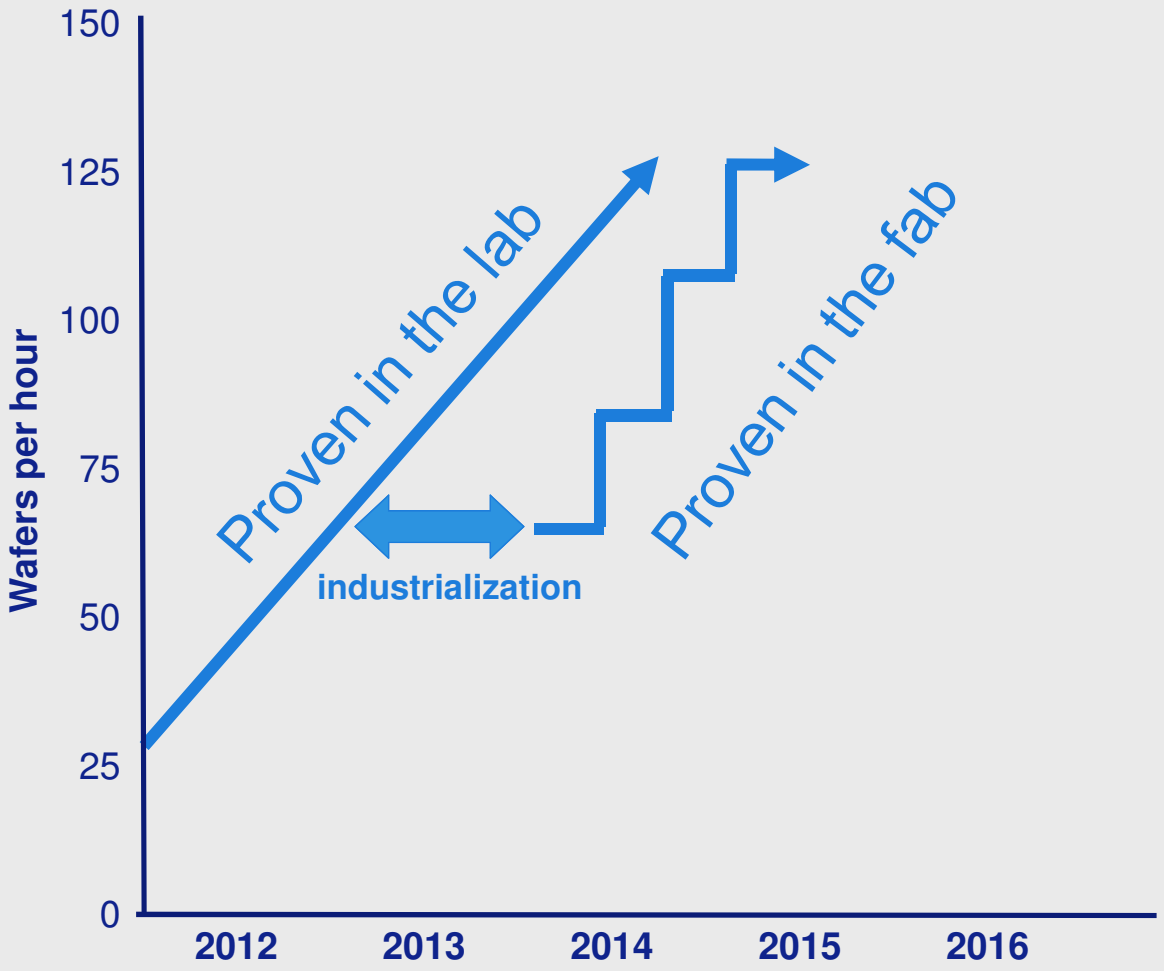


No change visible in far field image after $30X10^9$ pulses

Source: Cymer

ASML

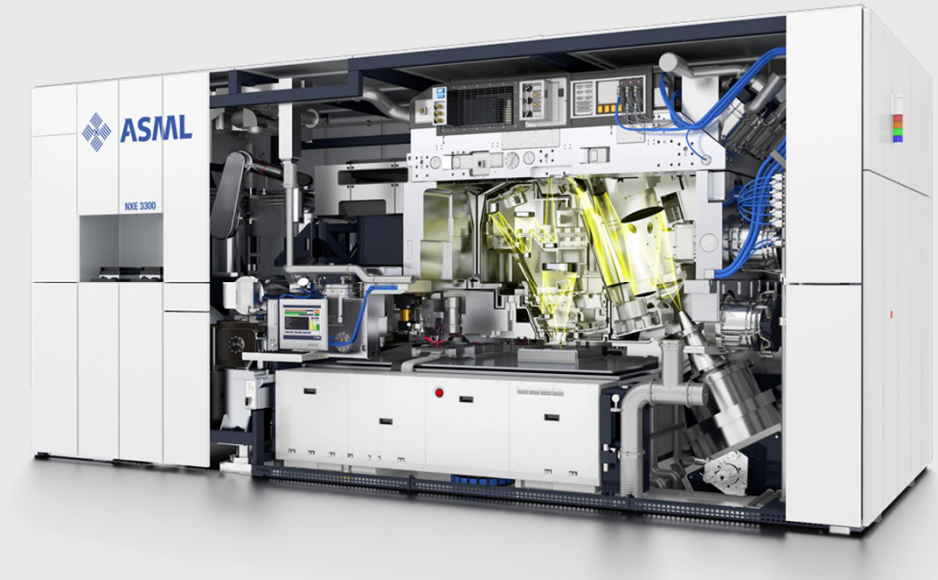
EUV industrialization in 2012 - 2014



Benefits for early NXE:3300 adopters:

- Stable performance:
  - 69 wafer/hour
  - resolution 22/18 nm
  - overlay (MMO) < 5 nm
- Reach 125 wafers per hour within two years.
- Add additional EUV layers with every productivity increase.
- Get more wafers out of same fab (smaller footprint).
- Remove design rule restrictions of DPT.
- Avoid overinvestment in ArFi and etch/deposition tools to support DPT.

NXE platform improving with NXE:3300B system



System performance	NXE:3300B
NA	0.33
Resolution (half-pitch)	22 nm (18 nm with OAI)
Overlay (DCO / MMO)	3.0 / 5.0 nm
Throughput	125 wph @ 15 mJ/cm^2

The NXE:3300B is a continuation of the NXE:3100 with

- system common modules: stages, handlers, sensors, electronics & software, a changed optical column
  - improved resolution (0.33 NA),
  - increased transmission for higher productivity at higher dose,
  - capability for off-axis illumination without energy loss,
- reduced footprint.

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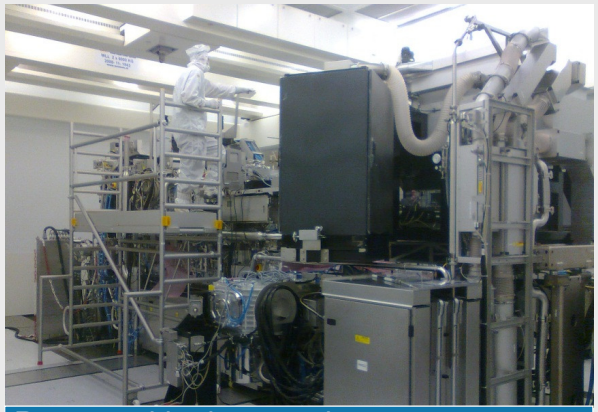
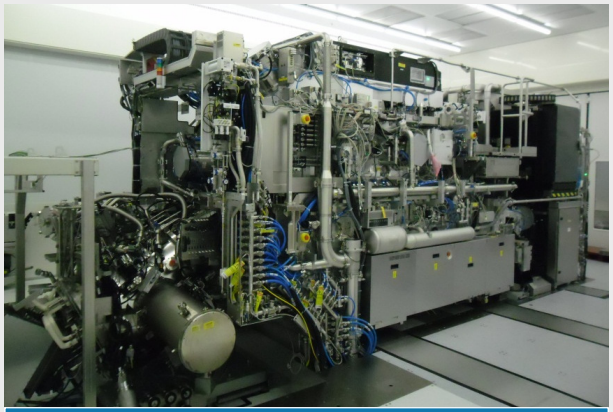
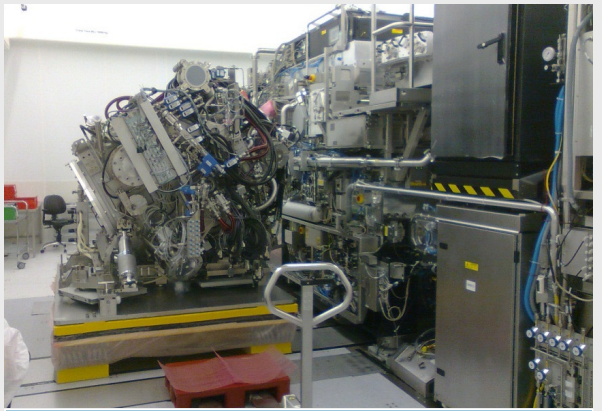
NXE:3300B integration status



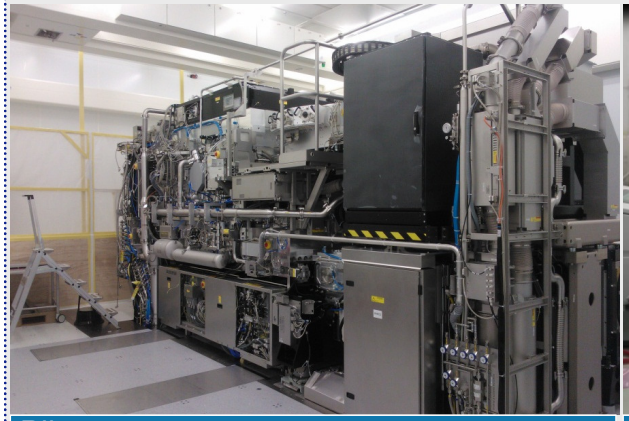
Proto 1 with sharp optics
First exposure in resist done
Coarse lens setup



Pilot 1 reliability testing
Cymer install and plasma qualification

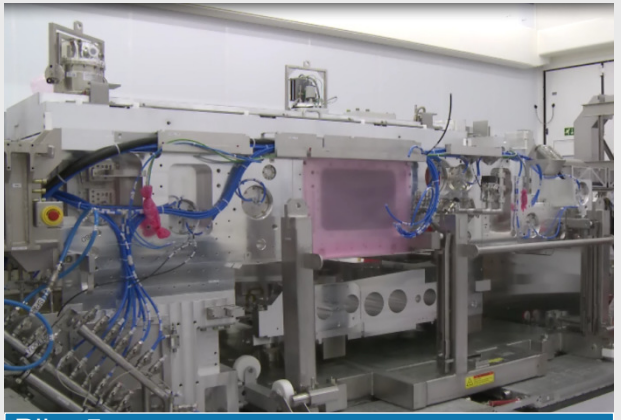


Pilot 2 reliability testing
Ushio source installation



Pilot 3
Dynamics performance testing

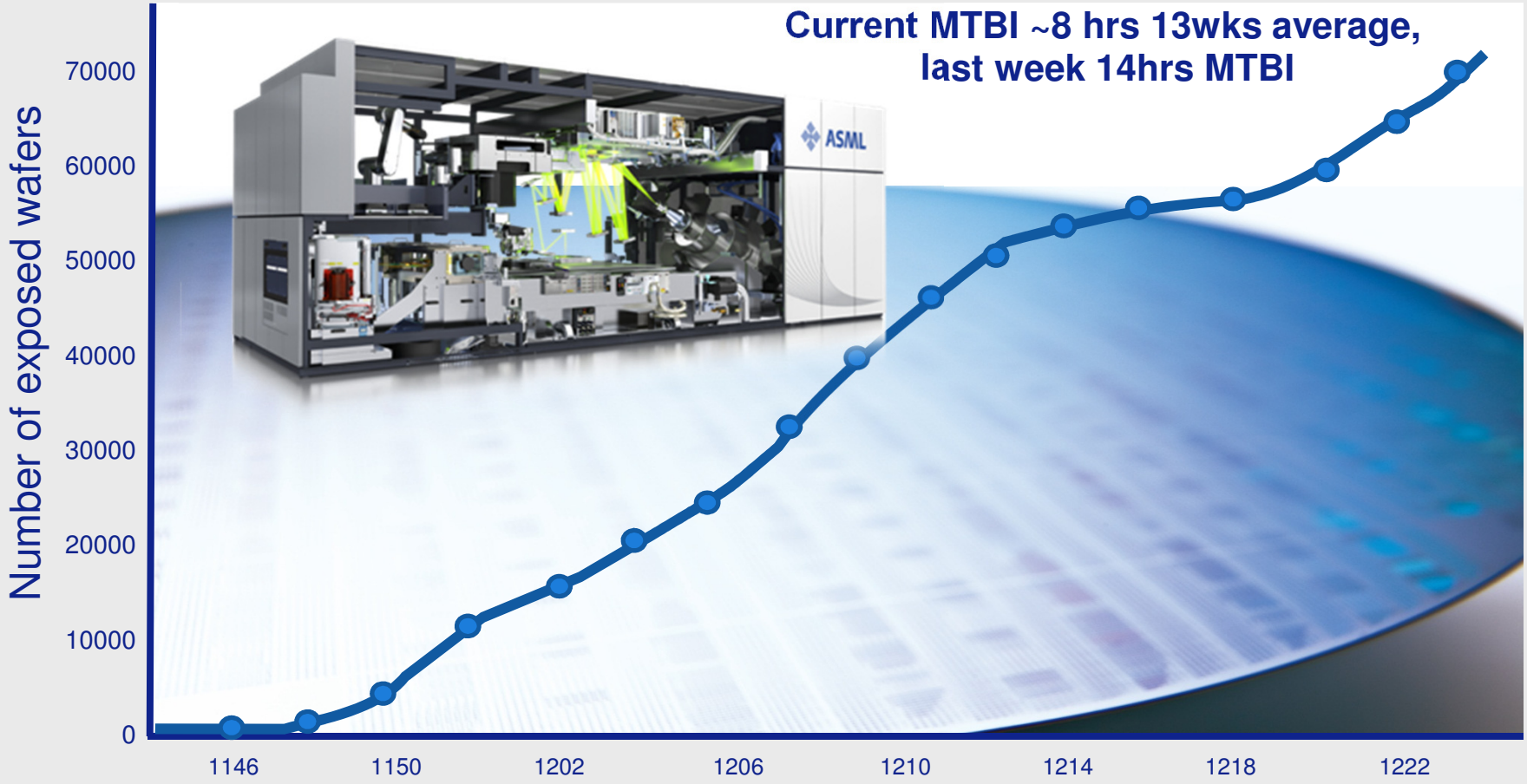
Pilot 4
Reticle handler installation



Pilot 5
Bottom module installation

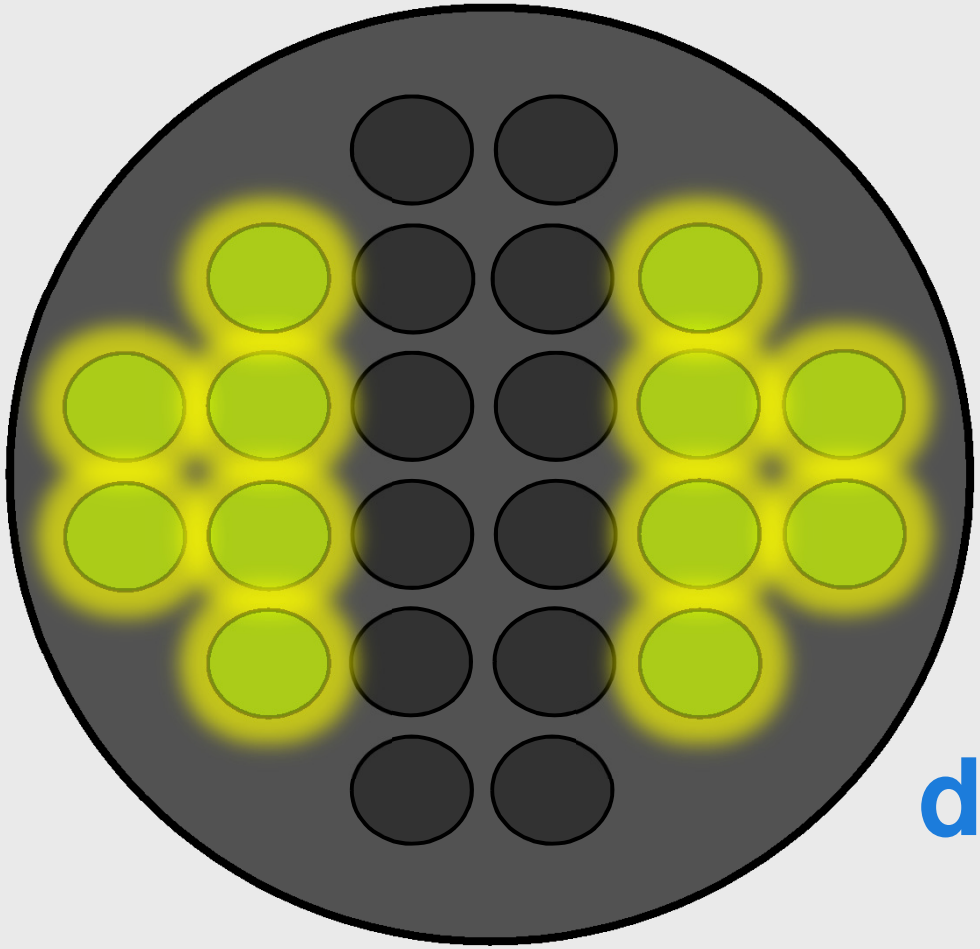
>70,000 wafers cycled through scanner body

>4,200 reticle exchanges performed



Extensive reliability testing ongoing on multiple NXE:3300B systems.

NXE:3300 illuminator design enables Off-Axis Illumination without energy loss

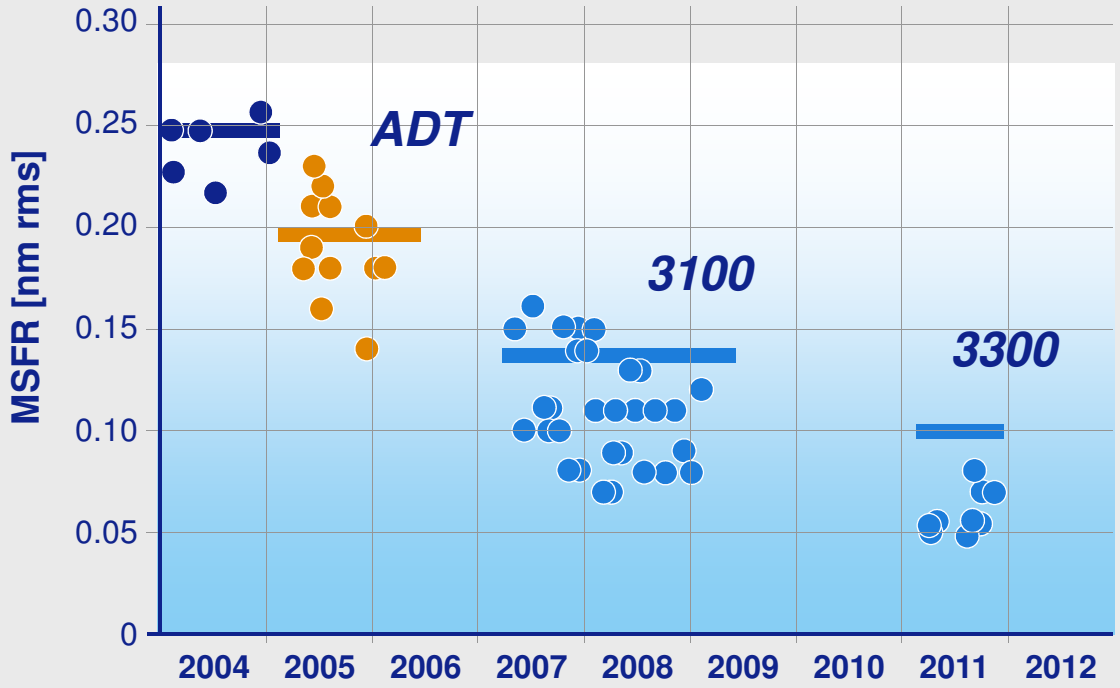


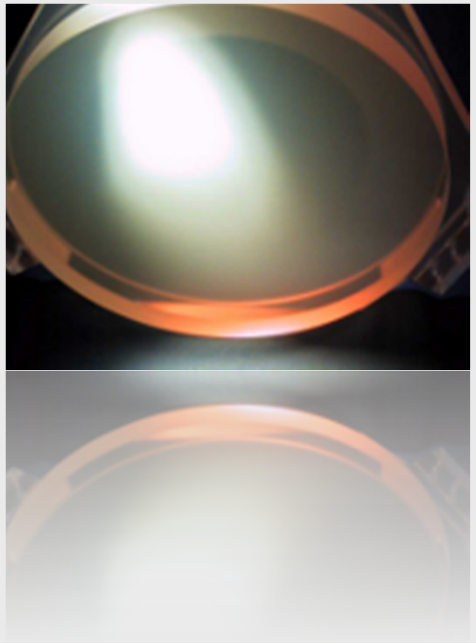
dipole x

source: Carl Zeiss SMT

ASML

NXE:3300B – first lens mirrors meet flare specs





	3100 average	3100 Champion	First 3300B mirrors
MSFR	102 pm	59 pm	78 pm 52 pm

First results on NXE:3300B mirrors well below the 6% flare specification (below a 2µm line) – based on these results ~4% can be expected.

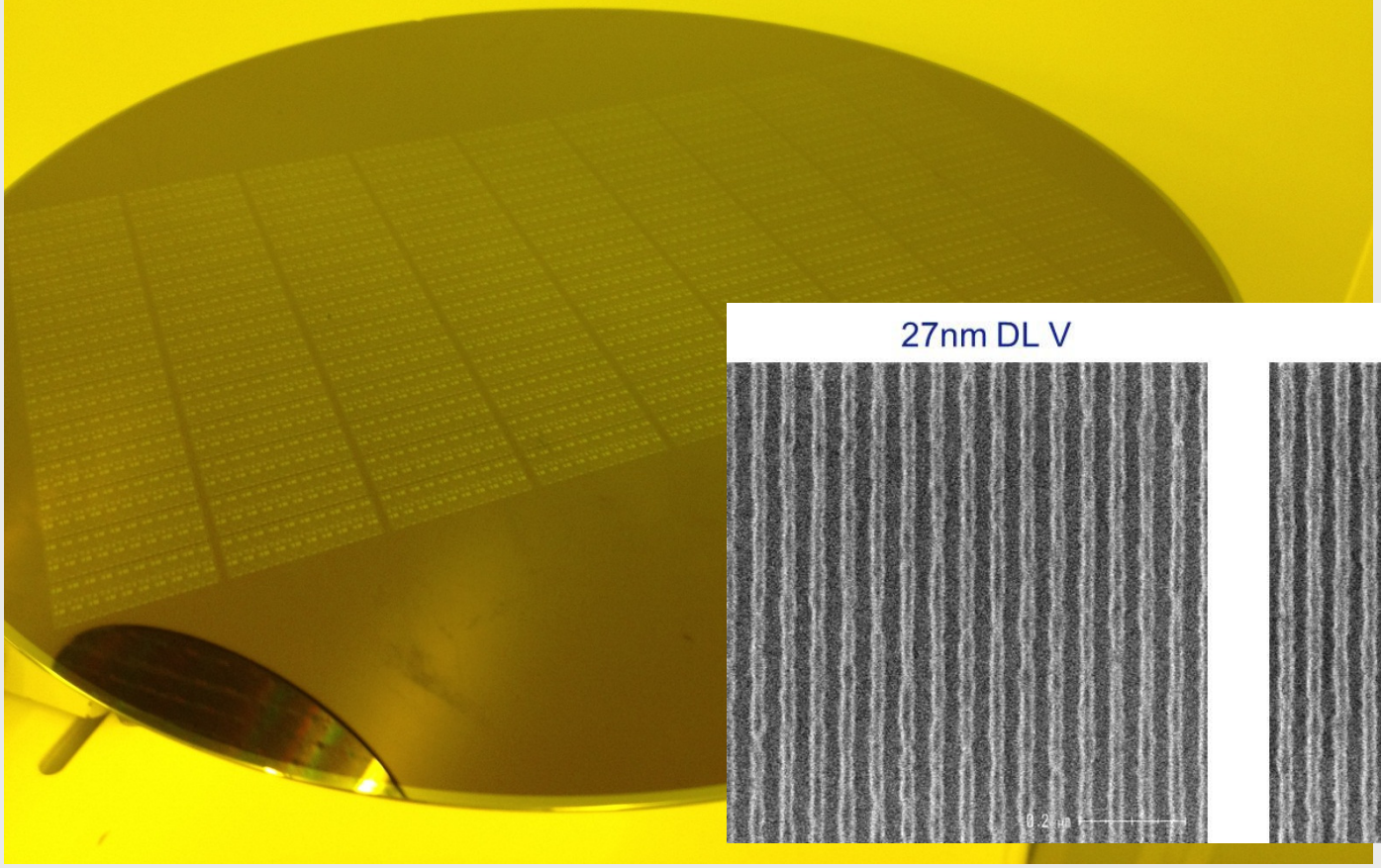
source: Carl Zeiss SMT

ASML


June 20th 2012
Scanner complete, source (LDP) operational,
mini-track interfaced, now exposing wafers…..

June 20th: NXE:3300B's first open-frame exposure

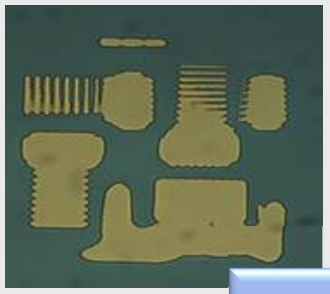
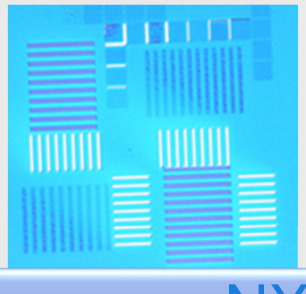
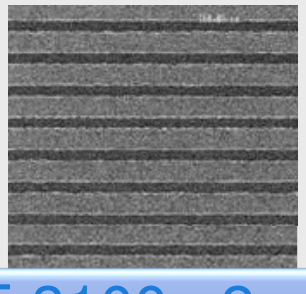
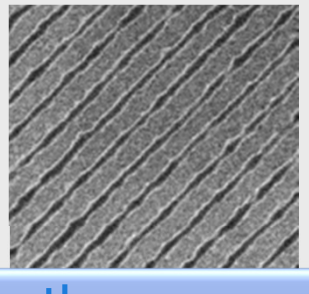
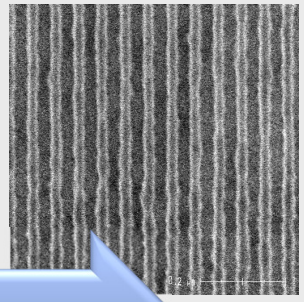
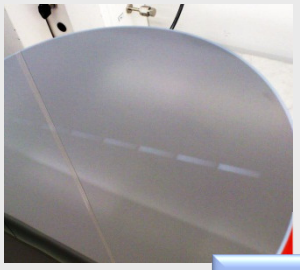
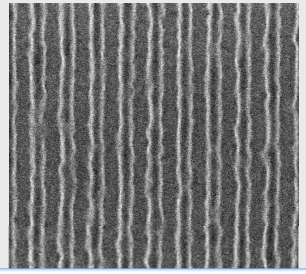
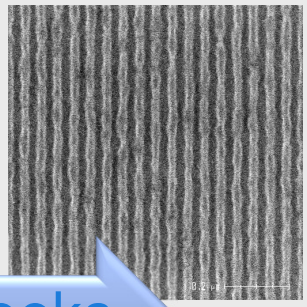
July 3rd: NXE:3300B's first FEM wafer !



Scanner setup not yet completed
(e.g., fading will be improved)

ASML

NXE Imaging setup progress: building a *platform* pays off

July 16 2010 First exposure	August 12 1.3 µm	August 26 250 nm	September 3 42 nm	September 26 27 nm
				
June 20 2012 First exposure	July 3 36 nm	July 4 25 nm		
				

NXE:3100 >2 months

NXE:3300B 2 weeks

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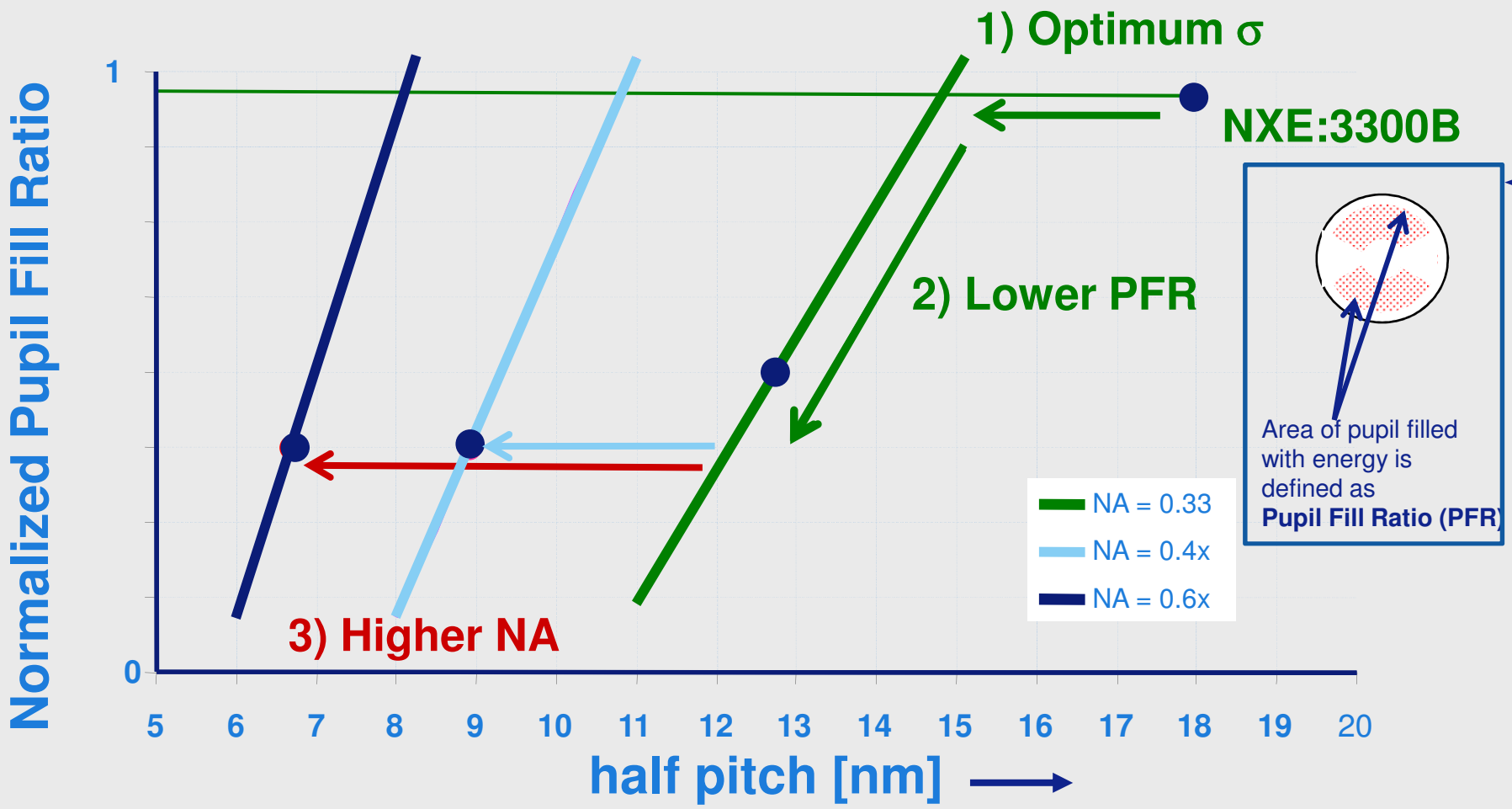
Content

- Why EUVL
- ASML EUV product roadmap
  - NXE:3100
  - NXE:3300
- Roadmap Extendibility

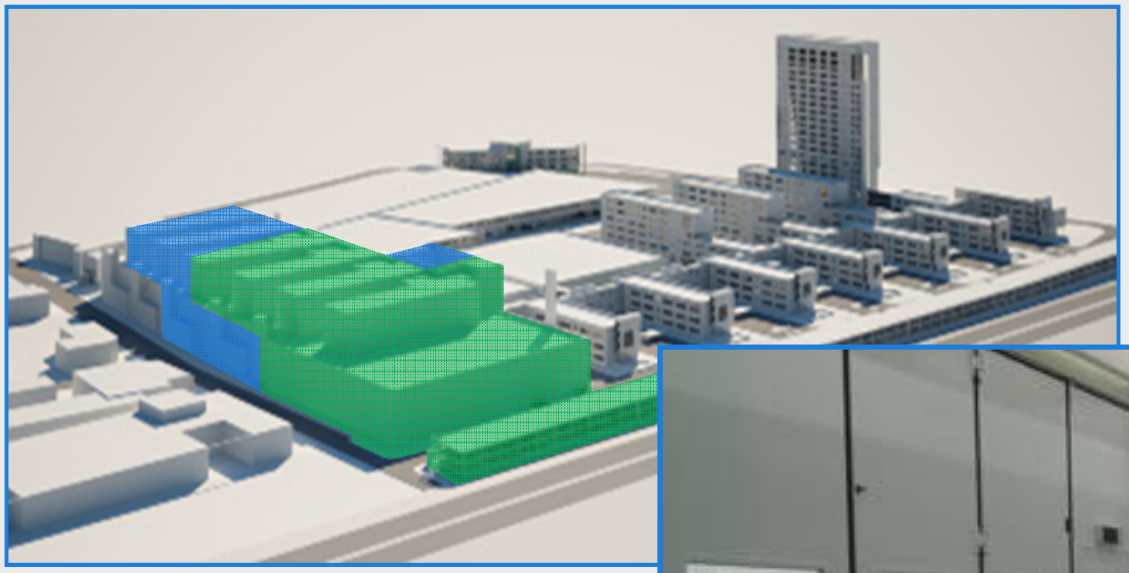
EUV in 3 steps to sub 10nm

First illumination optimization, then higher apertures



Building for volume production

New EUV fab at ASML for ~3x capacity increase



Existing EUV offices & manufacturing, 8 cabins.

New EUV offices & manufacturing,15 cabins.

Complete cleanroom finished: July ’12

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Summary & conclusions

- EUV has come a long way.
  - 2006: alpha-demo tools shipped
  - 2010: NXE:3100 (NA=0.25) pre-production tool shipped
  - 2012: NXE:3300B (NA=0.33) first exposures
- Further improvements are required on scanner (source), resist, and mask
- EUV can be extended multiple generations through combination of low-k1 and NA increase.

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